Hello again, it’s Ibrahim.

I will be explaining the test bench part of the code, which is the main driver code for the program, let’s get started.

First we’re including the ieee library to get std logic data type and numberic std

Then we’re defining an entity of the file.

And inside architecture we are defining a constant named “clock rate” which determines the frequency of the clock and a “cycle duration” constant which determines for how long the clock remains zero or 1.

the other variables here are signals for each state of both traffic lights.

And now we begin by creating an instance of our module and naming it tl\_module.

And on the next line we have a generic map and a port map which basically maps values from our module to local variables and signals, hence the name.

On the next line we have a statement that switches the value of signal my\_clock between 0 and 1 every half cycle\_duration.

Following that, we define our process which waits until there’s a rising edge, or until the value of my\_clock changes from 0 to 1 and when it does, it changes the value of reset flag, let’s open up the simulation and show you what this looks like.

\*open simulation\*

Alright, my partner will take it from here